Calculate

Ref ID	Assumption							
1	kw per electron volts	4.45E-26						
2	Assume battery kwatthr	80						
1	Electron volts per 80 KWHr	1.80E+27	1.7976E+27	Ref ID 6		Ref 1:		
1	basic charge electron/proton	1.60E-19				1cm = 1e7 nanometers		
3	Coluloms's constant ke	8.99E+09	Nm^2/C^2					
1	Electron Mass kilograms	9.11E-31						
8	Floating Gate Injected Electrons T-old	1.00E+05						
8	Floating Gate Injected Electrons T-new	1.00E+03						
Approx	Floating Gate Injected Electrons T-7.5v	1.00E+07						
10	Floating Gate Injected Electrons T-2011	5.00E+03						
	Devices needed T-old for 80 KWHr	1.80E+22						
	Devices needed T-new for 80 KWHr	1.80E+24						
	Devices needed T-7.5 for 80 KWHr	1.80E+20						
	Devices needed T-2011 for 80 KWHr	3.60E+23						
15	Swag Vfg based on Pulse Model	7.61E-01						
	Capacitance Total Swag	2.11E-19						
16	Amp equals Electron Volt	6.25E+18	Electrons per Second of Electron Flow					
	Reported Id Amp Delta Programming Floating Gate	Approx Amps						
17	Derived From Figure 2.5	1.00E-05		1.00E+04	1.50E+01	1.00E+04	1.00E+04	1.00E+04
18	Derived From Figure 2.2	1.00E-05						
18	Derived From Figure 2.10	1.00E-05						
18	Derived From Figure 3.2	1.00E-05						
18	Derived From Figure 3.5	1.00E-05						
	Electron Volts Stored in Floating Gate	6.25E+13		6.25E+22	9.38E+19	6.25E+22	6.25E+22	6.25E+22
	KW stored in Floating Gate/Cell	2.78E-12		2.78E-03	4.17E-06	2.78E-03	2.78E-03	2.78E-03
	Required Cells for 80 KW	6.46E+38		6.46E+29	4.31E+32	6.46E+29	6.46E+29	6.46E+29
		6.46E+38		6.46E+29	4.31E+32	6.46E+29	6.46E+29	6.46E+29

Reference	Action	View via Drain	Vsource	Vdrain	Vgate Pulsed Control	Vbulk	Vthreshold ref Control Gate	Vpinch Off
4	Adds electron to trap	Drain hot electron injection	0	<+5	9	UNK	UNK	
4	Remove electron from trap	Drain hot hole injection	X	<+5	-6	UNK	UNK	

5	Write: Add electrons to floating gate	Drain hot hole injection	0	0	+Voltage	0	shifts Pos	
5	Erase: Deplete electrons from floating gate	Drain hot hole injection	X	+HighV	0	0	shifts Neg	
9	Program Operation	Drain hot electron injection	0	18	0	UNK	UNK	
9	Erase Operation	Drain hot electron depletion	0	0	18	UNK	UNK	
10	Write: Add electrons to floating gate	Drain hot electron injection	20	20	5	UNK	UNK	
10	Erase Operation	Drain hot electron depletion						
11	Write: Add electrons to floating gate		X	+V	+LargeV	UNK	UNK	
11	Erase: Deplete electrons from floating gate		+V	X	-Voltage	UNK	UNK	
			Vsource	**Vdrain**	**Vgate Pulsed Control**	**Vbulk**	**Vthreshold ref Control Gate**	**VpinchOff**
12	Program: Select		3.3	3.3	-5.5	GND		
12	Program: Unselect		0	0	0	GND		
12	Program: Row Distrub		0	0	-5.5	GND		
12	Program: Column Distrub		3.3	3.3	0	GND		
12	Erase: Pre-erase		3.3	3.3	-5.5	GND		
12	Erase: Erase		-1.5	-1.5	5.5	GND		
12	Read: Select		0	0.4	1.1	GND		
12	Read: Unselect		0	0	0	GND		
13	Program: max		-V	-V	22	GND		
13	Program: min		-V	-V	18	GND		
13	Read between pulses							
13	Erase: Max Pulse with Read		+V	+V	-15V	GND		
13	Erase: Min Pulse with Read		+V	+V	-18V	GND		

Calculate

14	Programming		0	12	12	GND		
14	Erasing		n/c	0	12	GND		
	Write: Add electrons to floating gate		0	0	20	GND		
	Read Charge Quantity		0	0	Vref	GND		
	Erase: Remove electrons from floating gate		20	20	0	GND		

ID	Reference Title
1	google query dimension/quantity search string
2	Assumes 3200 pound vehicle similar to KIA Niro Ev 201 HP 64.8 KWHr Battery bumped to 80 KWHr
3	wikipedia search string for values
4	wikipedia: Charge trap flash drawings
5	Analysis and Modeling of Floating-Gate EEPROM Cells page 835 IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. ED-33, NO. 6, JUNE 1986
6	Metric-conversions.org Kilowatt-hours to Electron Volts
7	Haifa Abulaiha Programming of Floating-Gate Transistors for Nonvolatile Analog Memory Array Fig 2.5 Page 11
8	Direct charge measurement in Floating Gate transistors of Flash EEPROM using Scanning Electron Microscopy https://www.repository.cam.ac.uk/handle/1810/262365 page 1 right column
9	220722_1420_nvm_rom_eeprom_AN1837.pdf page 14 figure 11
10	Flash Memory - Changing Storage2011, page 1
11	Floating Gate Transistor: Why Flash Drive Density Will Stop Growing Next Year 2011 page 1.
12	A Highly Scalable Opposite Side Floating-Gate Flash Memory Cell, Table II. Using a modified Flash Memory design called Opposite-Side Floating Gate (OSFG). Note12.1 VdrainShared is the bias of the drain which is hsharing the same sources with the cell being considered.
13	NAND_Flash_101_ebook, page 7
14	Linux Flash for Newbies: Flash Memory Basics page 3,
15	A Comprehensive Simulation Model for Floating Gate Transistors. Figure 2.11 page 18.
16	https://www.mpoweruk.com/conversion_table.htm
17	Id to Vcg Plot Figure 2.5, page 11. Haifa Abulaiha, Programming of Floating-Gate Transistors for Nonvolatile Analog Memory Array see 220723-1710

18	Id to Vcg Plot Various Figures and pages as noted in usage., Steven J. Rapp A Comprehensive Simulation Model for Floating Gate Transistors see 220726_1542
19	Flassh Memory Integration, Jalil Boukhobza and Pierre Olivier, Figure 2.1

1.00E+04	
6.25E+22	
2.78E-03	
6.46E+29	
6.46E+29	
Additional Reference	

Ref ID 7	
Ref ID 7	
Vdrain Shared Note12.1	**Vread Gate**
3.3	1.65
0	1.65
0	1.65
3.3	1.65
3.3	1.65
-1.5	-1.5
0	1.1
0	0

Calculate
